EXHIBIT A

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, vs. STMICROELECTRONICS N.V., ET AL, Defendants.	6:21–CV–727-ADA JURY TRIAL DEMANDED

DECLARATION OF VIVEK SUBRAMANIAN, PH.D.

I, Dr. Vivek Subramanian declare as follows:

I. INTRODUCTION

1. I submit this Declaration concerning technical subject matter relevant to claim construction for U.S. Patent Nos. 7,498,633 ("the '633 Patent") and 8,035,112 ("the '112 Patent"). The facts and opinions stated in this declaration are true and of my own personal knowledge or investigation and as an expert in this field. If called to testify, I could and would testify to these facts and opinions, and any other facts that I become aware of after the filing of this declaration.

2. I am of legal age, and otherwise competent to make this declaration.

3. My name is Vivek Subramanian. I am offering this declaration in the above-captioned matter on behalf of STMicroelectronics, Inc. I am being compensated at my usual rate and my compensation is not dependent on any opinions that I may take in this matter, any testimony, or any intermediate or final resolution in the matter.

II. BACKGROUND AND QUALIFICATIONS

4. I received a bachelor's degree summa cum laude in electrical engineering from Louisiana State University in 1994. I received M.S. and Ph.D. degrees in electrical engineering, in 1996 and 1998, respectively, from Stanford University.

5. I am currently a Professor of Microtechnology at the École Polytechnique Fédérale de Lausanne (EPFL) (also known as the Swiss Federal Institute of Technology in Lausanne) in Switzerland. Until recently, I was also a professor of Electrical Engineering and Computer Sciences at the University of California, Berkeley. As of July 1, 2020, I have become an adjunct professor at UC Berkeley upon completion of my move to EPFL.

6. Throughout the course of my education, including my B.S., M.S., and Ph.D. degrees, I was involved in the design, fabrication, characterization, and modeling of semiconductor devices, including specifically devices designed for high voltage and high power applications. For example, I have designed high voltage transistors for operation of Flash memory devices using silicon, which have gone into commercial products, and have designed and fabricated high voltage wide bandgap devices for use in MEMS actuators based on zinc oxide.

7. After completing my Ph.D., I held multiple appointments simultaneously between 1998 and 2000. I served as a Consulting Assistant Professor in the Electrical Engineering Department of Stanford University. I also served as a Visiting Research Engineer in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, where my research focused on 25nm metal oxide semiconductor field effect transistor (MOSFET) design and fabrication. I worked on technologies for high-performance transistor processes, and I published several papers as a direct outcome of this technology development.

8. In 2000, I became an assistant professor at the University of California, Berkeley in the Department of Electrical Engineering & Computer Sciences. In 2005, I was promoted to the position of tenured Associate Professor, and in 2011, I was promoted to full Professor. In 2018, I became a full Professor of Microtechnology at EPFL in Switzerland, where I lead the Laboratory for Advanced Fabrication Technologies (LAFT). The lab focuses on the development and application of advanced additive fabrication techniques for realizing precision microelectronic and electromechanical systems. As of 2020, I have completed my move to EPFL and have therefore converted to an adjunct appointment at Berkeley.

9. My research has maintained a large effort on semiconductor devices, including working on various types of high voltage and high power devices, as mentioned above.

10. Starting in 2004, I was a founding technical advisor for Kovio. I led the development of Kovio's first commercial RFID tag product, including the design of both the tag and the reader, and including the development of the underlying proprietary transistor technology. This included the development of the materials, fabrication processes, and device design. My involvement with Kovio ended with Kovio's acquisition by thin film electronics, but Kovio continues to focus on this area.

11. I co-founded Locix Inc. in 2014. Locix develops and sells a range of wireless-enabled products, including proprietary Wi-Fi-based RF localization systems and sub-GHz low-power wireless sensor networks. As CTO of Locix, I led the development of the entire Locix RF product portfolio. I continue to be involved with Locix on a regular basis.

12. I have authored or co-authored over 200 technical papers in international journals and conferences and have been named an inventor or coinventor on more than 50 patents, many of which cover aspects of semiconductor device design and fabrication.

III. SUMMARY OF OPINIONS

13. I have been asked to provide an opinion about how a person of ordinary skill in the art would understand—or fail to understand—certain claim terms and teachings of the specifications of the ’633 and ’112 Patents. I understand that Defendants and Purdue have disclosed contentions for certain claim terms of these patent.

14. Of the claim terms that I understand are at issue for the ’633 Patent, I have been asked to provide my conclusions regarding the following:

a. preamble (claim 9)

b. less than about 3 micrometers (claim 9)

15. Of the claim terms that I understand are at issue for the ’112 Patent, I have been asked to provide my conclusions regarding the following:

a. a second, thicker oxide layer (claim 1)

b. a gate oxide layer (claim 6)

IV. LEGAL STANDARDS

16. I am not an attorney. However, the legal standards of claim construction and indefiniteness have been explained to me, and my understanding is as follows.

17. I have been informed about certain aspects of patent law, including claim construction. I am informed that claim construction is a matter of law. I am informed that patent claim terms should be given their ordinary meaning as they would be understood by a person of ordinary skill in the art (“POSITA”) having read the patent and understanding the full context in which the terms are used. First, a POSITA would consider the words of the claims that themselves. Second, the POSITA would turn to the patent specification to see if it sheds light on the meaning of the claims. A review of the prosecution history is also important. Third, the POSITA would turn

to extrinsic evidence, such as learned treatises, concerning relevant scientific principles, the meaning of technical terms, and the state of the art. Extrinsic evidence, such as dictionaries, articles or treatises, may also be useful, as long as it is considered in the context of the intrinsic evidence.

18. Further, I understand that a claim limitation is indefinite if the claim, when read in light of the specification and the prosecution history, fails to inform with reasonable certainty persons of ordinary skill in the art about the scope of the invention.

19. I have considered a number of materials in reaching my opinions in this declaration, including the ’633 Patent, its file history, the ’112 Patent, its file history, the parties’ respective claim construction disclosure statements, proposed constructions, and the evidence that they identified in the exhibits to the statements, as well as the parties’ respective identification of extrinsic evidence served on one another.

V. LEVEL OF SKILL IN THE ART

20. All of the opinions I express in this Declaration have been made from the standpoint of a person of ordinary skill in the field of the ’633 and ’112 Patents at the respective times of the inventions.

21. A POSITA for the ’633 Patent would have had the equivalent of a Bachelor’s degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of education, such as a Master’s degree, and vice versa. At the time of the claimed invention, I would have qualified as a POSITA under this standard.

22. A POSITA for the ’112 Patent would have had the equivalent of a Bachelor’s degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of

education, such as a Master's degree, and vice versa. At the time of the claimed invention, I would have qualified as a POSITA under this standard.

23. Although my qualifications and experience exceed those of the hypothetical person having ordinary skill in the art defined above, my analysis and opinions regarding the Patents-in-Suit have been based on the perspective of a POSITA at the time of the invention. Additionally, my opinions would not change if the hypothetical POSITA had somewhat more or less education or experience than what I outlined above, or if the subject matter of that education and experience was somewhat different.

VI. OVERVIEW OF THE '633 PATENT

24. The '633 Patent describes and claim 9 of the patent is directed to a semiconductor device referred to as a "double implanted metal-oxide semiconductor field-effect transistor," having a structure as shown in Figure 1. *See* '633 Patent at 3:7–8; 4:4-9; Figure 1.

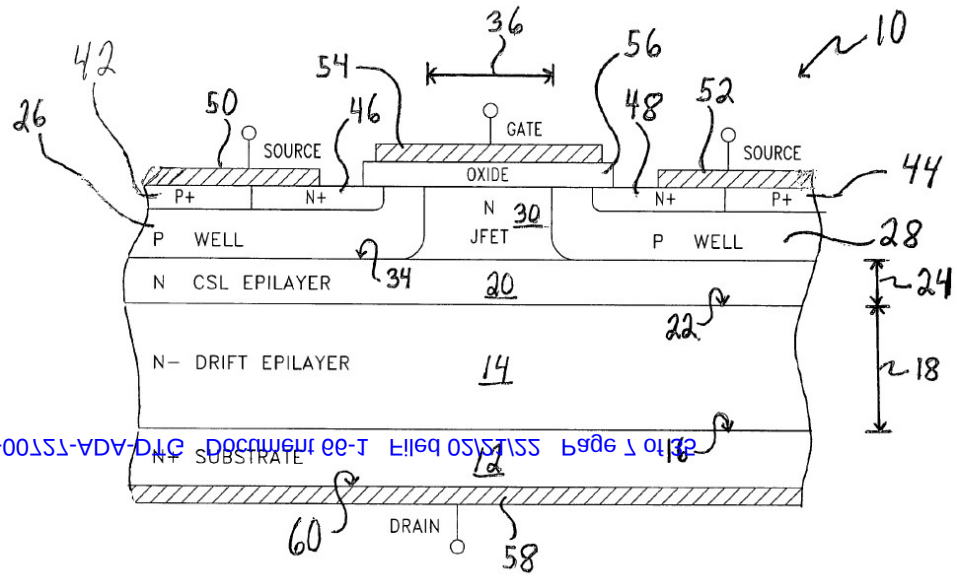

Fig. 1

25. Figure 1 of the '633 Patent shows a cross-section (i.e., a cut-away side view) of the device. As shown in Figure 1, the device of the '633 Patent includes a drain, 58, a substrate, 12, a

drift layer, 14, and an optional current spreading layer 20 (CSL). *Id*. at 2:59-66; 3:16-22. The '633 Patent explains that above the drift layer "[t]he semiconductor device 10 also includes two doped semiconductor wells or base regions 26, 28," labeled "P WELL," that "are doped with a P-type impurity to a 'P' concentration." *Id*. at 5:23–24, 5:42–43. Above the "P WELLs" and drift layer are source metallic electrodes 50, 52, a "GATE," 54, and a dielectric layer 56, labeled "OXIDE."

26. Under the gate and between the wells 26 and 28 is an area labeled "JFET," 30. *Id*. at 5:25–26, 6:3–5.

27. A POSITA would understand the operation of a vertical metal-oxide semiconductor field-effect transistor such as is shown in Figure 1 of the '633 Patent. As shown below in a marked version of Figure 1, when an appropriate voltage is applied to the gate, current is able to flow between the sources and the drain, through the JFET region 30. As a result, the vertical metal-oxide semiconductor field-effect transistor is able to be used as a switch, turning current flow on and off. More specially, a POSITA would understand that a field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor.

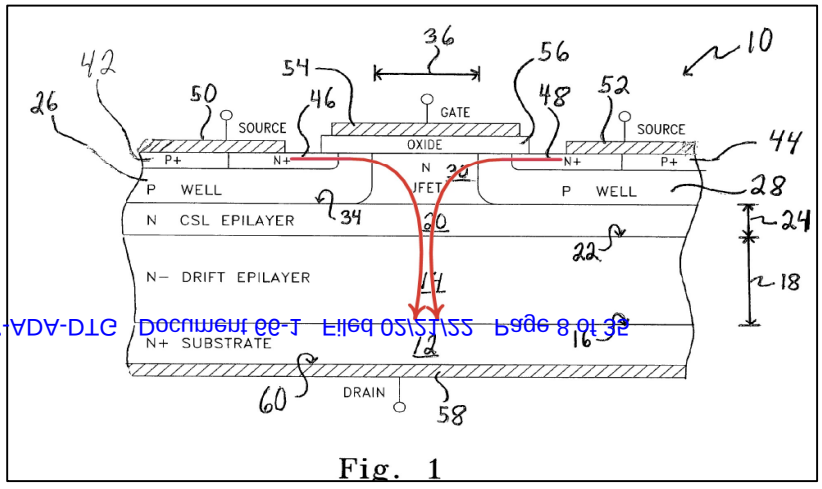

Fig. 1

VII. DISPUTED CLAIM TERMS OF THE '633 PATENT

A. Whether the preamble of claim 9 is limiting

28. I am informed that a preamble to a claim is limiting when it provides antecedent basis for terms in the claim, or it breathes life and meaning into the claim.

29. In my opinion, as explained below, the preamble of claim 9 is limiting because it breathes life and meaning into the claim because it defines what is being claimed when the individual limitations of the claim are otherwise incomplete.

30. Specifically, as explained below, the preamble of claim 9 provides important context for the overall claim because it defines what is being claimed when the other individual limitations of the claim are otherwise incomplete. The preamble informs what type of device is being addressed and it necessarily fills in blanks or missing pieces in the configuration such as a gate, gate insulator and drain, which are essential components of a metal-oxide semiconductor field-effect transistor that are not listed in any of the limitations in the body of claim 9.

31. A POSITA would understand that there can be many different configurations, but a field effect transistor generally includes at least a source, a drain, gate and substrate. A MOSFET would also have a source, gate, drain and substrate elements and also include a gate insulator.

32. As shown in claim 9, which is reproduced below, by informing what type of device is being addressed, the preamble also provides context with regard to the possible arrangements and cooperation of the elements of the claim.

> 9. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
>
> a silicon-carbide substrate;
>
> a drift semiconductor layer formed on a front side of the semiconductor substrate;
>
> a first source region;
>
> a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
>
> a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
>
> a second source region;

a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;

a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

33. As can be seen in claim 9, the relative arrangement and cooperation of some of the elements is undefined. For example, the claim is silent regarding the position of the first and second source regions and whether the source regions have any connection or cooperation with other claim elements. The claim does not say whether the source regions are in, on, between, or even in contact with either the substrate or drift semiconductor layer. The preamble, however, by identifying the type of device as a double-implanted metal-oxide semiconductor field-effect transistor, provides context regarding how the components can be arranged so as to result in a field-effect transistor, rather than something else.

34. The preamble of claim 9 also recites a "double-implanted device." From a review of the specification of the '633 Patent, without the preamble a POSITA would not conclude that the device claimed is double-implanted. The specification states that "The MOSFET ***may be*** a double-implanted MOSFET (DMOSFET)." *Id*. at 2: 26-27 (emphasis added). In support of this, a POSITA would note that the preamble of claim 1 of the '633 Patent does not recite "double implanted." Similarly, a POSITA would note that the specification states that "Illustratively, the

semiconductor device 10 is a vertical double implanted metal-oxide semiconductor field-effect transistor (DMOSFET). However, in other embodiments, the semiconductor device 10 may be embodied as other types of MOSFET devices." *Id*. 4:6-11.

35. Accordingly, in my opinion, because the patent asserts that different types of devices are within the scope of the disclosure, a POSITA would conclude that the preamble of

claim 9 provides important context because it more specifically defines the type of the device to which the claim is directed when the other limitations of the claim are incomplete, do not specifically define the arrangement or cooperation of the elements, or otherwise define the type of the device.

B. "less than about 3 micrometers"

36. In my opinion, as explained below, the phrase "less than about 3 micrometers" as used in claim 9 of the '633 Patent fails to inform, with reasonable certainty, a POSITA as to the scope of that term.

37. Specifically, the literal words of the phrase do not express precise boundaries on the scope of the term regarding either the upper or lower boundaries of the JFET width, and neither the specification of the '633 Patent nor the subject matter at issue provides a basis for determining the scope of the phrase with reasonable certainty.

38. The specification of the '633 Patent does not say what the "less than about 3 micrometers" width is supposed to achieve. As a result, there is no basis from which to determine the range of values encompassed by the claim or the precision required. Instead, the '633 Patent explains that there are multiple characteristics that a designer may consider. "One design consideration … is the blocking voltage of the semiconductor device. [F]or high-voltage power applications, a high blocking voltage is generally desirable. Another design consideration … is the specific on-resistance." *Id.* 1:18-28. And the specification explains that "the design of the semiconductor device 10 involves a number of parameters that may affect or be interdependent upon each other. As such, the design process of the semiconductor device 10 may include a number of reiterative steps of selecting a width 36 and a doping concentration for the JFET region 30, selecting a doping concentration and a thickness for the current spreading layer 20, selecting a

doping concentration and a thickness 18 for the drift layer 14, and/or selecting values for other parameters to achieve the desired characteristics of the semiconductor device 10." *Id*. at 6:55-62.

39. A POSITA would know that the different parameters of a MOSFET, including the width of the JFET region, would create design tradeoffs. "In addition to the resistance of the MOS inversion layer, the specific resistance of the DMOSFET also includes the resistance of the JFET region between the implanted p-base regions. This introduces a tradeoff in the design: As the spacing between base regions is increased to reduce the JFET resistance, the area of the device also increases, increasing R_{SP} [specific resistance]. In addition, as the spacing increases, and the effectiveness of the base regions in terminating the electric field in the blocking state diminishes, increasing the field in the oxide and lowering the blocking voltage." James A. Cooper, Michael R. Melloch, Ranbir Singh, Anant Agarwal & John W. Palmour, "Status and Prospects for SiC Power MOSFETs," in IEEE Transactions on Electron Devices, Vol. 49, No. 4, pp. 658–64 (Apr. 2002) p 659.

40. The specification states "In some embodiments, the JFET region 30 is also fabricated to have a short width 36 relative to a typical DMOSFET device, which may reduce the specific on-resistance of the semiconductor device 10." *Id*. 6:21-24. To the extent a POSITA could infer the scope of "less than about 3 micrometers" by comparing it to a "typical DMOSFET," the specification is unclear what is meant by a "typical DMOSFET" device. Specifically, the specification does not explain whether the "typical DMOSFET devices" refers to a power or logic MOSFET, a vertical double implanted metal-oxide semiconductor field-effect transistor, or some other type of DMOSFET. Likewise, the specification does not identify the technology of the "typical DMOSFET." The specification and claims of the '633 Patent may purport to cover

DMOSFETs made with silicon carbide substrates (*see e.g.*, claim 1) as well as DMOSFETs not limited to silicon carbide substrates (*see e.g.*, claim 12).

41. To the extent a "typical DMOSFET" refers to a silicon carbide MOSFET like claim 9, silicon carbide DMOSFETs around the time of the invention of the '633 Patent do not show a "typical" width for a JFET region. In a patent issued around the time of the application for the '633 Patent for a silicon carbide power MOSFET, JFET widths of 1-10μm were reported. *See* U.S. 6,956,238B2 (Ryu '238) at 6:53-55. In a 2002 article on silicon carbide MOSFETs, JFET widths between 2-5μm were evaluated by simulation and it was reported that "if the JFET gap is too small, specific on-resistance increases significantly." Sei-Hyung Ryu, Anant K. Agarwal, Nelson S. Saks, Mrinal K. Das, Lori A. Lipkin, Ranbir Singh & John W. Palmour, "Design and Process Issues for Silicon Carbide Power DiMOSFETS," in Mat. Res. Soc. Symp. Vol. 640, pp. H4.5.1 – H.4.5.6 (2001) (hereafter "Ryu article") at H4.5.2. Based on these articles and my own knowledge and experience, what the '633 Patent means when it refers to a "typical DMOSFET" is unclear. As a result, any attempt at comparison between the claimed JFET width of less than about 3 micrometers and that of a "typical DMOSFET" does not provide a basis for better understanding the scope of the claim term.

42. Although the patent explains there are many parameters to trade off, neither the specification nor claim 9 specifies any particular combination of design parameters, such as thickness or doping concentrations for any layer, that would influence or inform what is within the claimed range for the JFET width. Instead, the specification explains that the JFET width and other parameters are dependent on the subjective personal choice of the designer because they are selected "to achieve the desired characteristics of the semiconductor device." *Id*. at 6:61-62. The Ryu '238 Patent likewise confirms that the JFET width is subjective in a silicon carbide MOSFET

and “The particular gap utilized for a given device may depend upon the desired blocking voltage and on-state resistance of the device.” Ryu ’238 at 11:23-25. Accordingly, because the desired characteristics of the semiconductor device are subjective and the particular JFET width depends on the personal choice of the designer, there is no way for a POSITA reading the ’633 Patent to know from the patent the boundaries of this claim element.

43. Likewise, the subject matter at issue does not provide a basis for determining either the upper or lower end of the range “less than about 3 micrometers” with reasonable certainty. At the lower end, the phrase “less than about 3 micrometers” would appear to literally include any dimension down to zero width. But the ’633 patent does not disclose how to make operable vertical DMOSFETs at all possible dimensions down to and including zero JFET width and if the JFET was reduced to zero width, the device would no longer be a vertical double diffused MOSFET since the device would not be functional to control the flow of current between the source and the drain via alteration of the gate field.

44. At the upper end, the phrase “less than about 3 micrometers” appears intentionally vague as to what it intends to cover without a reason for being vague. The ’633 patent does not say there is any particular characteristic or purpose of the device that is achieved with a JFET width in the vicinity of less than 3 micrometers that is not achievable at other dimensions. Accordingly, there is nothing about the purpose that the "less than about three micrometers" limitation serves from which to determine how large the JFET width can be in the claimed invention and still serve that purpose. Instead, from the ’633 Patent, a POSITA would understand that the term at issue is simply a dimension. As such, if the inventor had wanted to include 3 micrometers within the claim, instead of saying “less than about three” the inventor could have written “less than or equal to 3 micrometers.” Likewise, if the inventor had wanted to set the upper

bound at 2.5 micrometers, 3.5 micrometers or 4.0 micrometers—or any other dimension—it was possible to do so clearly and without vagueness.

VIII. OVERVIEW OF THE '112 PATENT

45. The '112 patent is generally directed to "high voltage power MOSFETs," 2:24–26, and the patent describes a vertical MOSFET, having a structure generally as depicted in Figure 3, which is reproduced below. *Id*. at 1:44; 2:49–50, 3:60–63, Figure 3:

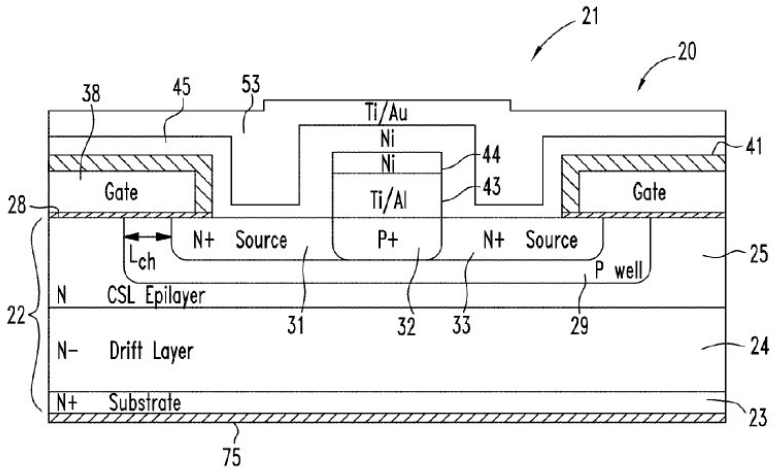

FIG. 3

46. The MOSFET of Figure 3 includes a silicon-carbide (SiC) wafer having a substrate body 22, which includes a substrate 23 and a drift layer 24 formed on substrate 23. *Id*. at 4:8–11. Figure 3 illustrates the MOSFET with an optional current spreading layer (CSL) 25 formed on drift layer 24. *Id*. at 4:25–26, 4:28–30. Polycrystalline silicon (*i.e.*, polysilicon) gates 38 are formed on the upper surface 28. *Id*. at 4:66–5:2. Each gate 38 is "surrounded along its top, bottom, left and right sides by an insulating layer of silicon dioxide 41." *Id*. at 5:2–10. Although the '112 patent also describes forming a Ti/Al contact metal 43, and a Ni contact metal 44 atop the P+ base 33 (*see* center of Figure 3 above), none of these features are claimed by the '112 patent.

47. A contact metal layer 45 is "formed over the entire MOSFET 21, overlapping the polysilicon gate 38, but insulated from it by the thick oxide 41 on the top and sides thereof." *Id*.

at 5:5–8. The contact metal 45 forms an electrical connection with the source regions 31, 33. *Id.* at 5:18-25.

48. In particular, the ’112 Patent and the structure of the MOSFET of the invention of the ’112 Patent purportedly address a problem with conventional DMOSFETs where the source contact may be unintentionally or unavoidably misaligned with respect to the gate and source regions in the device substrate. The ’112 Patent explains the problem with the conventional DMOSFET starting with Figure 1. *Id.* 3:25-48, Fig. 1. Specifically, Figure 1 shows a “perfectly aligned,” conventional DMOSFET, where the source contact is “defined by photolithography, and source contact 13 must be separated from the edge of the gate 14 by sufficient distance X so that source contact 13 and gate 14 cannot touch even under worst-case misalignment of the source contact mask.” 3:26-31. As shown in Figure 1, when the structure is “perfectly aligned,” the cross-hatched Ni metal source contact 13 is centered and evenly spaced between the two gates.

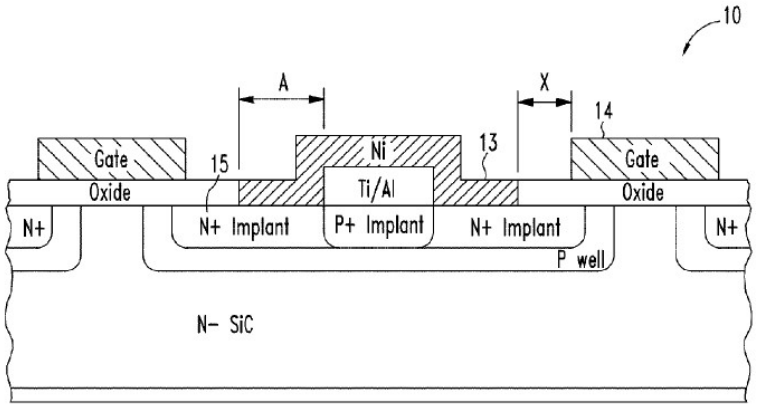

FIG. 1

49. A POSITA would understand that “defined by photolithography” refers to a common process used in forming semiconductor structures. Conventionally, photolithography uses light and a photomask to define structures or shapes to be formed in the device.

50. Defining and forming structures with photolithography is a multistep process that may start with creating a photomask having a geometric pattern of transparent and opaque areas that depict the structures to be formed on the device in a particular step or at a particular layer. The partly fabricated semiconductor device is coated with a photosensitive material typically called photoresist, the photoresist is dried, and light is projected through the photomask onto the photoresist coated device to illuminate the areas of the device that correspond to the transparent regions in the photomask transferring the geometric pattern to the light sensitive layer. The light causes chemical reactions in the photoresist in the illuminated areas and the photoresist is subsequently developed to fix in the photoresist layer the pattern defined by the illuminated areas. The developed photoresist layer is then chemically treated to selectively remove the portions of the photoresist layer that were either illuminated or not. A POSITA would also recognize that the developed and patterned photoresist layer may be referred to as a "mask" and that the resulting patterned photoresist layer can then be used in subsequent steps to form structures on the device. For example, if the patterned photoresist layer was formed on top of a layer of insulating material, the patterned photoresist layer, i.e., mask, could be used as a shield in a subsequent step of etching the insulating material so that portions of the insulating layer would be etched (removed) in areas where there is no overlying photoresist layer and the insulating material would not be removed in the areas where it is covered (or masked) by the patterned photoresist. Alternatively, the patterned photoresist layer may be used like a stencil enabling deposition of a new layer of material in the shape of the exposure pattern upon the device. Fabrication of a semiconductor device often involves many photolithography steps as layers of structure are built up on the device. As a result, it is necessary to correctly align the photomask and partly fabricated device during each photolithography step to that the structures formed correctly align to each other.

51. The ’112 Patent illustrates and describes a conventional DMOSFET with worst-case mask misalignment in Figure 2. *Id*. 3:48-59. The patent explains “That is, if the MOSFET design parameters require that source metal 13 never gets closer to gate 14 than spacing Y, even under a worst-case mask mis-alignment (as shown in FIG. 2), then the target mask alignment must be performed with a spacing X.” *Id*. 3:48-52.

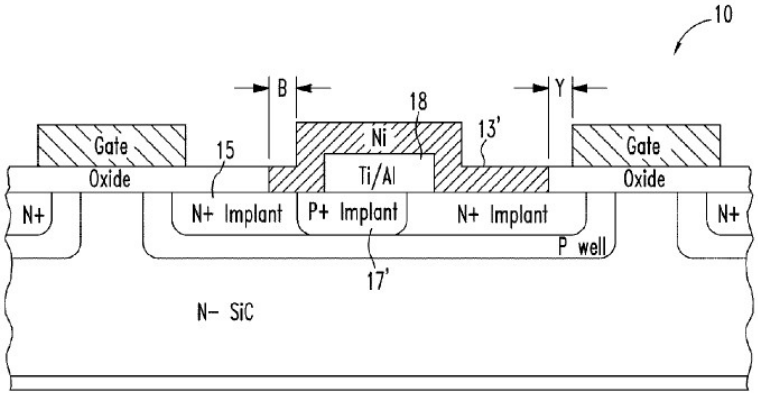

FIG. 2

52. As shown in Figure 2, in the case of “worst-case misalignment” the cross-hatched Ni metal source contact 13’ is off center to the right and, at the right edge thereof, there is only a small space Y remaining between the source contact and the gate. If the source contact 13’ was even further misaligned to the right and was to actually touch the gate, a short-circuit would result and the device would likely be ruined. Likewise, at the left edge of the source contact 13’ there is only a small overlap “B” between the source contact and the N+ implant 15 that forms the source region, whereas the source contact 13’ is supposed to overlap the N+ implant 15 that forms the source.

53. A POSITA would understand that when the patent refers to the “worst-case misalignment” it is referring to the amount of misalignment that is possible or potentially expected as a result of the precision of the particular tools, machines or processes that will be used in the

manufacture of the device. Such tools or machines may enable alignment of the mask and device to only within a certain tolerance for mechanical or other reasons, and that perfect alignment is not always possible. A POSITA would understand that the patent is describing that a designer would need to take the maximum misalignment possibility into account when designing the device, for example in deciding the size and spacing between elements. And the patent explains that the size of the device may, as a result, be larger than otherwise desired: "The necessary additional spacing (which is the difference between X and Y) unduly increases the area of the cell, and thus increases RON, SP." *Id*. 3:52-55.

54. The problem that the '112 Patent purports to solve is the risk of mis-alignment and the corresponding necessity in a conventional DMOSFET structure to build in extra size or space to accommodate misalignment, despite the fact that doing so may result in undesirable things such as, for example, increases in RON, SP (i.e., specific on-resistance). The '112 Patent explains "Both these problems—increased contact resistance at reduced area overlap B from mask misalignment and increased cell width to ensure adequate spacing Y—are eliminated in the present invention by negating the opportunity for misalignment of source contact metal and gate." 3:55-59.

55. The '112 Patent explains that the present invention negates the opportunity for misalignment of source contact metal and gate because it uses an insulation layer over the gate of the type formed, created or grown by reacting the gate material without using any mask. *Id*. at 6:20-7:11; 7:20-33. The '112 patent shows and describes this layer with respect to Figure 7. "Referring to FIG. 7, after the ion etch creates gates 38, an oxidation layer 68 is grown over the entire upper surface of intermediate semiconductor product 58a." *Id*. 6:20-23.

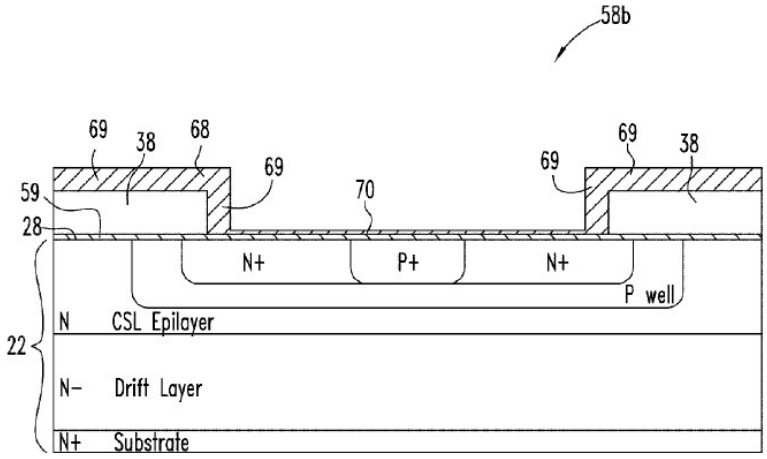

FIG. 7

56. As explained below with respect to the disputed claim terms, by using this type of insulating layer, the patent describes "the area of the functional source contact is not determined by the alignment of any masking levels and is not subject to random misalignments during processing. Instead, it is totally determined by the spacing between adjacent polysilicon gates and is, in fact, self-aligned to the gate level, being separated by the thickness of the oxide layer covering the gate. This eliminates the alignment tolerance (X or Y in FIGS. 1 and 2), thus reducing the cell area and the specific on-resistance." *Id*. 6:63-7:4.

IX. DISPUTED CLAIM TERMS OF THE '112 PATENT

57. The phrase "a second, thicker oxide" is recited in claim 1 of the '112 Patent and the phrase "a gate oxide" is recited in claim 6 of the patent.

58. I am informed that STMicroelectronics has proposed that the phrase "a second, thicker oxide" in claim 1 of the '112 Patent means "an oxidation layer formed, created or grown by reacting the gate, thicker than the first oxide layer," and the phrase "a gate oxide" in claim 6 means "an oxidation layer formed, created or grown by reacting the gate." In my opinion, as explained below, the constructions proposed by STMicroelectronics are accurate because, among

other reasons, they describe the type of oxide that results from a reaction with the material of the gate that makes an oxidation layer, which is an essential aspect of the invention, as opposed to a deposited type oxide layer, for example, deposited using TEOS or by CVD, which is contrary to the invention.

59. Similarly, I am informed that Purdue has proposed that the phrases "a second, thicker oxide" in claim 1 and "a gate oxide" in claim 6 both mean "layer of oxide that is on the tops and sides of each gate and that is thicker than the layer of oxide below each gate." As explained below, in my opinion the constructions proposed by Purdue are incorrect because, among other reasons, the construction does not require an oxidation layer type of oxide made by a reaction with the material of the gate and, instead, appears intended to include a deposited type of oxide layer, which is contrary to the invention.

60. A POSITA would conclude from the '112 Patent, the problem to be solved, and the prosecution history that the "second, thicker oxide" recited in claim 1 of the '112 Patent and the "a gate oxide" recited in claim 6 of the patent refer to the same structure, which is an insulating layer made of oxide over the top and sides of the gates. The patent explains and illustrates that this insulating layer, shown as 68 in Figure 8, insulates the gate from the subsequently deposited metal contact that makes electrical connection to the N+ source regions and P+ region.

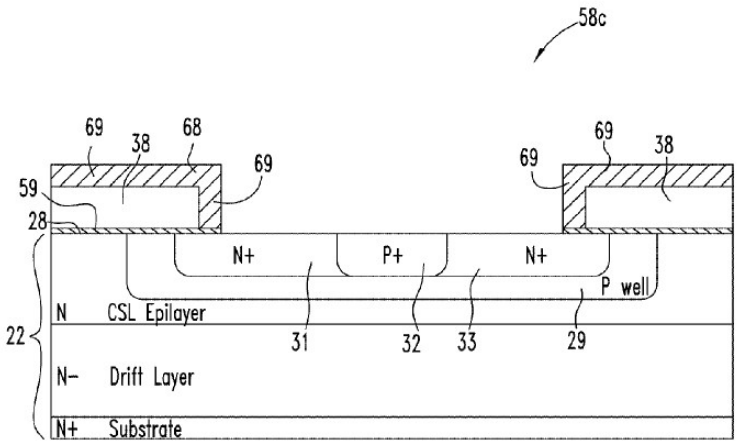

FIG. 8

61. As I explain, there is nothing in the '112 Patent or its prosecution history that suggests to a POSITA that these two terms are intended to have different meanings or refer to different structures. To the contrary, while the two terms use different words, both claims 1 and 6 expressly identify the location of the layer. In claim 1 the layer is "over each of said gates and the sides thereof" and in claim 6 the layer "over said tops and sides of each of said gates."

62. A POSITA would also recognize that, in claim 6, the patentee is coining its own term when it uses phrase "gate oxide" to refer to the layer over the gate. A POSITA would know the expression "gate oxide" has a standard and well-known meaning the art of field effect transistors as the thin insulating layer ***under the gate*** between the gate and the channel region in the substrate. *See e.g.*, B. Jayant Baliga, Modern Power Devices (1987) ("The gate bias modulates the conductivity of the channel region by the strong electric field created normal to the semiconductor surface through the oxide layer. For a typical gate oxide thickness of 1000 Å and gate drive voltage of 10 V, an electric field of 106 V/cm is created in the oxide") and p. 332, Fig. 6.52(a) (showing a cross section with gate oxide labeled); Dethard Peters, Reinhold Schörner, Peter Friedrichs & Dietrich Stephani, "4H-SiC Power MOSFET Blocking 1200V with a Gate

Technology Compatible with Industrial Applications," in Materials Science Forum Vols. 433-436, pp. 769–72 (2003) passim and Fig. 1; Michael Quirk & Julian Serda, Semiconductor Manufacturing Technology (2001) p. 632 — Glossary ("gate oxide The thin layer of thermal oxide that separates the gate electrode (terminal) from the channel region of the semiconductor substrate."); U.S. Patent No. 7,622,741 at 4:1-2, Fig. 1 ("Gate oxide films 5a, 5b and gate electrodes 6a, 6b are provided on then—type SiC semiconductor epitaxial layer 2."); U.S. Patent No. 7,645,658 at 1:42-44, Fig. 1 ("On the channel layer 4, a gate oxide layer 8 is formed at least to cover upper surfaces of the channel regions of the channel layer 4"); U.S. Patent No. 8,133,787 at 16:52-56, Fig. 14 ("A gate oxide film 68 having a thickness of, e.g., 110 nm and using the portion of the surface area of the channel epitaxial layer 64 located over the p-type base regions 63 as a channel 55 region is formed so as to cover at least the surface of the channel region").

63. The specification of the '112 Patent uses the term "gate oxide" consistent with the standard practice. For example, the patent describes "These steps to fabricate intermediate semiconductor product 58 include growing the 50 nm thick silicon lower gate oxide layer 59 on top of the entire surface 28 of the SiC substrate body 22 by thermal oxidation in a pyrogenic oxidation system at 1150° C. for 2.5 hours." *Id*. at 5:47-51. However, in claim 6 of the '112 Patent, a POSITA would recognize that patentee is using the term "gate oxide" differently and contrary to standard usage. As a result, a POSITA would look to the entirely of the patent to determine what the term "gate oxide" in claim 6 refers to. In my opinion, a POSITA would conclude "gate oxide" refers to the same structure that is called a "second, thicker oxide layer" in claim 1, because, among other reasons, the claim requires the layer to be over the gate and there is no other oxide over the gate described in the patent.

64. A POSITA would conclude from the '112 Patent, the problem to be solved, and the prosecution history that the purported invention of claims 1 and 6 is a MOSFET with an oxidation layer over the tops and sides of the gates that is formed, created or grown by reacting the gate material. This enables forming the source contact positioned correctly with respect to the gates where, as the '112 Patent describes, "the area of the functional source contact is not determined by the alignment of any masking levels." *Id*. 6:63-65.

65. A POSITA would have this understanding because, among other reasons, a POSITA would note the specification of the patent repeatedly describes the invention as a MOSFET with "self-aligned source contact." *See, id.* at title ("SiC Power DMOSFET with Self-Aligned Source Contact."); 1:21-23 ("This invention relates generally to semiconductor field effect transistors, and more particularly to field effect transistors having self-aligned source contacts."); 2:24-26 ("The present invention provides high voltage power MOSFETs, with self-aligned source contacts and a method for making the same."); 6:63-7:4 ("the functional source contact is not determined by the alignment of any masking levels … and is, in fact, self-aligned to the gate level.").

66. More specifically, a POSITA would understand that the specification describes a particular type of insulator (a grown-type) as an essential component in creating the self-aligned source contact without using any mask, "Referring to FIG. 7, after the ion etch creates gates 38, an oxidation layer 68 is grown over the entire upper surface of intermediate semiconductor product 58a." *Id*. at 6:20-22. "The foregoing oxidation growing step 16d grows oxidation on the polysilicon gates 38 about ten times faster or more than on the SiC substrate (on which there is already about a 50 nm oxidation layer 59). Consequently, oxidation layer 68 on top and on the

sides of each gate 38 has grown to about 500 nm thick (at 69), while only about 10 nm or less of oxidation are added to upper substrate surface 28 (at 70)." *Id*. at 6:27-32.

67. A POSITA would likewise understand the type of insulating layer described in the '112 Patent (i.e., in the case of an oxide, an oxidation layer formed, created or grown by reacting the gate) is essential to the invention because the '112 patent explains it "tak[es] advantage of the fact that polysilicon forms a much thicker SiO_2 layer than does SiC when thermally oxidized at temperatures in the 850-1000° C. range. The SiO_2 is then removed over the SiC by a short etch, without using a photomask to define the area where the oxide is removed and expose the N+ implants 31 and 32 and the P+ base 33." *Id*. at 5:65-7:4. "Because it is much thicker, the oxide over the polysilicon gate is not completely removed during this process and forms an insulating layer over and around the polysilicon gate 38." *Id*. at 6:1-4.

68. A POSITA would recognize when the SiC and polysilicon gate are "thermally oxidized," that forms an oxidation layer which is a type of oxide formed, created or grown by reacting the gate. This is similar to what happens to a piece of iron left outside to rust. In that case, oxygen in the air or in water reacts with the iron and a surface layer of iron is oxidized so that rust (i.e., rust is iron oxide) grows on the surface.

69. More generally, an oxide layer in a semiconductor—such as a silicon oxide which is a compound of silicon and oxygen (SiO_2)—can be either a deposited type of oxide or it can be a grown type of oxide. As one textbook on semiconductor manufacturing describes, "Oxide on a silicon wafer is created by either the grown or deposited method. A grown oxide layer occurs on a wafer by providing externally supplied high-purity oxygen in an elevated-temperature environment to react with the silicon substrate… A deposited oxide layer is generated by using an external silicon source and O_2 and reacting these materials in a chamber to form a thin film on the

wafer surface." *See,* Michael Quirk & Julian Serda, Semiconductor Manufacturing Technology (2001) ("Quirk"), p. 225. As shown in the figure below, in a grown oxide a portion of the exposed area of the silicon substrate is consumed by the reaction and is converted into silicon oxide. Quirk, p. 233. In the figure, the oxide thickness t is greater than the thickness 0.45t, which is the thickness of the amount of silicon consumed.

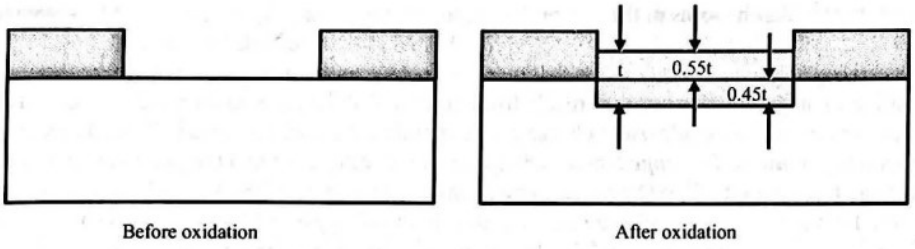

FIGURE 10.8 Consumption of Silicon During Oxidation

70. A POSITA would also recognize when the '112 Patent describes that the SiC and polysilicon gate are "thermally oxidized," that description is not describing a deposited type of oxide layer. A POSITA would have an understanding of grown oxides and that oxide growth on silicon occurs faster than on silicon carbide and that the growth of oxides is described in various textbooks and articles. *See e.g.*, A. S. Grove, Physics and Technology of Semiconductor Devices (1967) pp. 22-31 (disclosing "In industrial practice, silicon dioxide layers are most frequently formed by the thermal oxidation of silicon through the chemical reaction Si(solid) + O_2 → SiO_2(solid) or Si(solid) + $2H_2O$ → SiO_2 (solid) + $2H_2$" and also disclosing formula that model the rate of growth of the oxide layer with time.); S. M. Sze, Physics of Semiconductor Devices (2d Ed. 1981) pp. 98-106 (disclosing oxidation reactions and rate of silicon oxide growth.); Y. Song, S. Dhar, L. C. Feldman, et al., "Modified Deal Grove Model for the Thermal Oxidation of Silicon Carbide," in Journal of Applied Physics, Vol. 95, No. 9, pp. 4953–57 (May 1, 2004); pp. 4953-57 (disclosing reaction equations and rate of growth of silicon oxide on silicon carbide.). A POSITA

would also understand there is a difference between grown and deposited layers. *See e.g.*, S. P. Murarka, M. Eizenberg & A. K. Sinha, Interlayer Dielectrics for Semiconductor Technologies (2003) pp. 1-35 (describing types of insulating layers) and pp. 121-155 (describing silicon-based dielectrics); Michael Quirk & Julian Serda, Semiconductor Manufacturing Technology (2001) (comparing Chapter 10 "Oxidation" pp. 225-525 with Chapter 11 "Deposition" pp. 257-294).

71. A POSITA would also understand that the invention of the '112 patent relies on the fact that the silicon carbide substrate and polysilicon gate form, create or grow oxide at different rates and that this difference in growth rate is how the invention creates an oxide over the top and sides of the gate while it is able to selectively expose the areas of the source surface without using any mask, in order to provide for the metal source contact layer 13 to make electrical contact.

72. Specifically, the '112 Patent illustrates and describes this sequence starting with Figure 5 where the individual gates are defined using a mask. The patent explains that Figure 5 shows "an intermediate semiconductor product 58 with all substrate, layers and doping fabricated up through top SiC surface 28 (which together constitute substrate body 22), an oxidation layer 59, a 4000 Å thick layer 66 of polysilicon formed across oxidation layer 59, and application of gate mask 62 atop polysilicon layer 66 in preparation for etching away a portion of polysilicon layer 66 to create gates 38." *Id*. at 5:27-31.

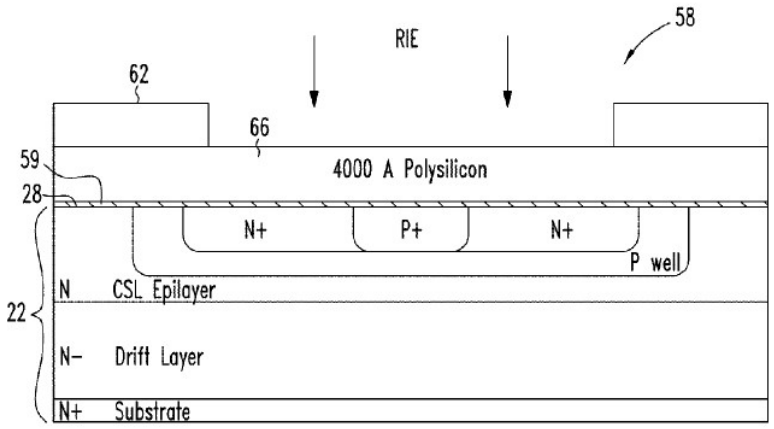

FIG. 5

73. A POSITA would understand that Figure 5 shows an intermediate semiconductor product and that an intermediate semiconductor product is a partially but not completely fabricated device and that depicting an intermediate semiconductor product may help to explain the invention. A POSITA would understand that Figure 5 shows an intermediate semiconductor product with a 4000Å thick layer of polysilicon 66 and mask 62 on top of portions of the polysilicon layer. A POSITA would understand that there are two masks shown in Figure 5, one on the top left labeled 62 and a second on the top right that is not labeled. The figure shows downward arrows with the legend "RIE," which a POSITA would understand refers to "reactive ion etch"—a type of dry etching that bombards the surface with high-energy ions to etch away material.

74. A POSITA would understand Figure 6 of the patent to show the intermediate semiconductor product after the etching indicated in Figure 5, where "Removal of the gate mask reveals the intermediate semiconductor product 58a shown in FIG. 6." *Id*. at 5:58-60. As shown in the figure, the etching performed with a mask (i.e., gate mask 62) has removed the portion of the polysilicon layer that was not covered by the gate mask so as to create individual gates 38 shown on the left and right sides of the figure.

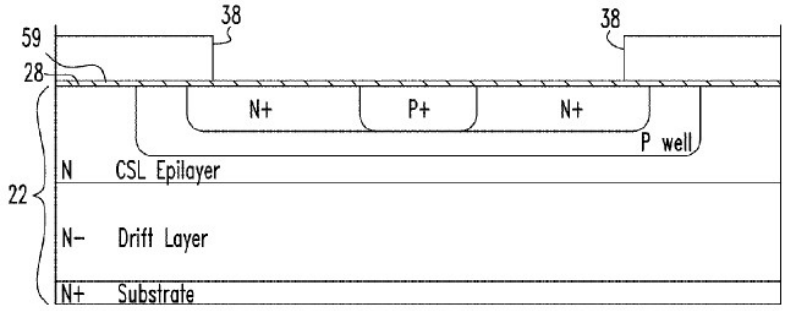

FIG. 6

75. A POSITA would understand that the '112 Patent next describes that the intermediate device is thermally oxidized to grow an oxidation layer over the top and sides of the polysilicon gate and that at the same time a thinner oxide also grows over the N+ source regions and P+ region. The patent describes, "Referring to FIG. 7, after the ion etch creates gates 38, an oxidation layer 68 is grown over the entire upper surface of intermediate semiconductor product 58 a (Appendix II, step 16, the third step "d": Dry oxidation for 6 hrs. at 1000 C in tube 7, then wet oxidation for 4.5 hrs at 950 C and then dry oxidation for 2 hrs at 950 C) to produce intermediate semiconductor product 58 b. Oxidation layer 59 grown from the SiC surface 28 is about 50 nm thick. The foregoing oxidation growing step 16 d grows oxidation on the polysilicon gates 38 about ten times faster or more than on the SiC substrate (on which there is already about a 50 nm oxidation layer 59). Consequently, oxidation layer 68 on top and on the sides of each gate 38 has grown to about 500 nm thick (at 69), while only about 10 nm or less of oxidation are added to upper substrate surface 28 (at 70)." *Id.* at 6:20-34.

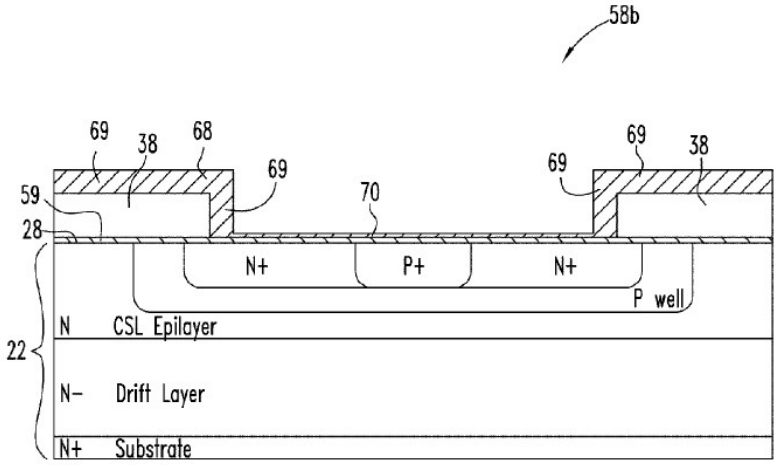

FIG. 7

76. A POSITA would understand an oxidation layer grown over the entire upper surface of intermediate semiconductor product of the type resulting from "Dry oxidation for 6 hrs. at 1000 C in tube 7, then wet oxidation for 4.5 hrs at 950 C and then dry oxidation for 2 hrs at 950 C)" is a grown type of oxide layer, not a deposited type of oxide layer. And a POSITA would understand the oxide layer over the tops and sides of the gates is "an oxidation layer formed, created or grown by reacting the gate," which is polysilicon material. The thin oxide layer over the N+ source regions and P+ region (the center region of the figure) is an oxidation layer formed, created or grown by reacting the substrate, which is silicon carbide material.

77. A POSITA would also understand that because the grown oxidation layer over the gates is thicker than the layer over the N+ source regions (because polysilicon oxidizes faster than silicon carbide), it is possible to perform etching ***without a mask*** in order to expose the N+ source regions by removing the oxide layer over those regions while still leaving the gates covered with an oxidation layer. The '112 Patent describes this saying "The SiO_2 is then removed over the SiC by a short etch, without using a photomask to define the area where the oxide is removed and expose the N+ implants 31 and 32 and the P+ base 33." *Id*. at 5:65-7:4. "Because it is much thicker,

the oxide over the polysilicon gate is not completely removed during this process and forms an insulating layer over and around the polysilicon gate 38." *Id.* at 6:1-4.

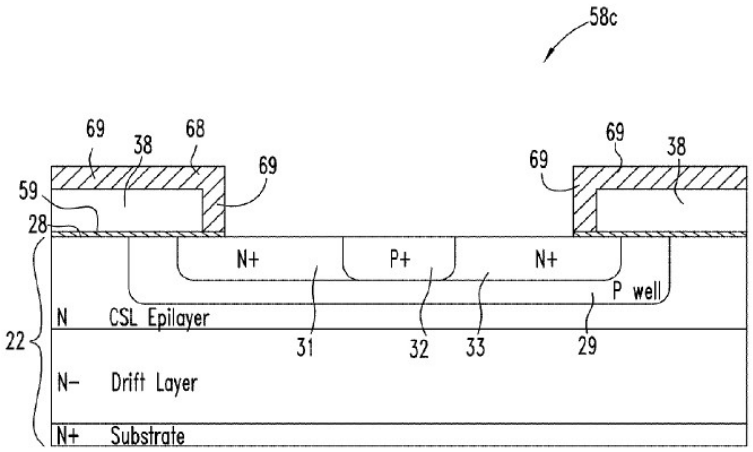

FIG. 8

78. A POSITA would likewise understand that when the '112 Patent is describing etching "without a mask," it is describing that the etch would attack the entire top surface of the intermediate device which includes both the oxidation layer 68 over the gates as well as the oxidation layer over the N+ Source regions and P+ region because there is no mask to limit etching to select areas. This is in contrast, for example, to what is shown and described with respect to Figure 5 where gate masks 62 protect portions of the polysilicon layer from the RIE etch and prevent etching of the polysilicon in these covered areas.

79. A POSITA would likewise understand that if a deposited oxide layer was used instead of an oxidation layer formed, created or grown by etching the gate, the deposited oxide layer would have the same thickness over both the tops of the gates and the upper substrate surface 28 where the N+ source regions and P+ region are located. A POSITA would understand a deposition of an oxide layer would not result in different thicknesses of the deposited oxide layer

over the gate and substrate surface simply because the gate material is polysilicon and the substrate material is silicon carbide.

80. From the ’112 Patent, a POSITA would also conclude that the use of a grown type insulating layer (i.e., in the case of an oxide, an oxidation layer formed, created or grown by reacting the gate) is not merely an example or embodiment of the invention, but an essential feature of the inventions of claims 1 and 6 of the patent. A POSITA would also recognize that claims 1 and 6 of the ’112 Patent expressly require either an “oxide layer” or a “gate oxide.” Accordingly, a POSITA would understand that the insulating material relevant to construction in claims 1 and 6 are “oxides” rather than some other type of insulating material.

81. For the reasons already explained, a POSITA would find relevant that the specification of the ’112 Patent describes the “present invention” saying “Both these problems—increased contact resistance at reduced area overlap B from mask misalignment and increased cell width to ensure adequate spacing Y—are eliminated in the present invention by negating the opportunity for misalignment of source contact metal and gate.” 3:55-59. A POSITA would recognize that the only solution in the patent where the opportunity for misalignment is negated is by using a grown type layer so that “the area of the functional source contact is not determined by the alignment of any masking levels and is not subject to random misalignments during processing. Instead, it is totally determined by the spacing between adjacent polysilicon gates and is, in fact, self-aligned to the gate level, being separated by the thickness of the oxide layer covering the gate. This eliminates the alignment tolerance (X or Y in FIGS. 1 and 2), thus reducing the cell area and the specific on-resistance.” *Id*. 6:63-7:4. A POSITA would find the descriptions particularly informative because they are said to describe the “present invention.”

82. Further, a POSITA would conclude that the patent expressly excludes any alternative embodiment that does not use a grown type insulating layer where it says "Alternative embodiments are contemplated wherein the secondary steps (and even certain of the primary steps) can be performed in ways other than recited, with materials, solutions and concentrations other than recited, and for times and under temperatures and conditions other than recited, so long as the gate and substrate source (or other ohmic contact materials) react to form, create or grow an insulation layer (such as SiO2) sufficiently faster, larger and/or with more insulating capacity at the gate surface than at the substrate surface and that will therefore be uniformly removable at a rate which will remove all such formed, created or grown layer substantially or entirely completely from the substrate surface and leave a sufficiently insulative layer around the gate." *Id*. 7:20-33. From the above, a POSITA would understand the specification to say that any alternative embodiment different from the specific examples described in the patent must use a grown type insulating layer (e.g., in the case of an oxide, an oxidation layer formed, created or grown by reacting the gate) with a gate material and substrate material that grow at different rates so that a uniform etch can be used. A POSITA would likewise understand this to be describing etching performed without a mask because it is relying on the insulating layers having different thicknesses over the gate versus over the substrate surface and that the layers are "uniformly removable." And, as already described, a POSITA would understand that a deposited oxide would not have the same effect because a deposited oxide would have the same thickness over the gates and substrate surface so that uniform etching without a mask would not allow the N+ source regions and P+ region to be uncovered while the top and sides of the gates remain sufficiently covered.

83. A POSITA would also recognize from the prosecution history that with regard to the "gate oxide" term the patentee argued (with regard to what is now claim 2) "In connection with

the other limitations of claim 4, applicant's invention provides for a SiC substrate and polysilicon gates because growth of the oxidation layer on the polysilicon gates occurs considerably faster than on the SiC substrate, which creates a much thinner combined oxide layer between adjacent gates (as shown in Fig. 7 of the application) than is simultaneously formed on the tops and sides of such gates. Thus, after a short oxide etch is applied, long enough to completely remove the thin, combined oxide layer over the substrate surface (and between the gates), there is still left a very thick insulating oxide layer on the tops and sides of gates. This is more than an obvious design choice and is nowhere disclosed, taught or suggested by Miura." Response dated May 23, 2001, at p. 12. A POSITA would recognize that the argument above is describing, as "applicant's invention," a grown oxide layer with different growth rates on the polysilicon gate and silicon carbide substrate. A POSITA would also recognize that the claim limitation in claim 2 of the patent (addressed by the argument above) is identically phrased as the corresponding limitation of claim 6, and the identical claim language in view of the argument described above, is another reason why a POSITA would conclude that the "gate oxide" term is an oxidation layer formed, created or grown by reacting the gate.

84. A POSITA would also recognize that while column 7 lines 20-33 of the '112 Patent refers to "an insulation layer (such as SiO_2)," the disputed terms in claims 1 and 6 of the '112 Patent expressly require either an "oxide layer" or a "gate oxide." Accordingly, a POSITA would understand that the insulating material that cover the tops and sides of the gates in claims 1 and 6 are "oxides" and that an oxide is a type of insulating material. For that reason, a POSITA would understand that "an oxidation layer" "formed, created or grown by reacting the gate" is an accurate construction for the disputed terms of the '112 Patent.

85. I reserve the right to supplement my opinions in the future to respond to any arguments that Purdue raises and to take into account new information as it becomes available to me. I also reserve the right to provide additional opinions related to other case issues.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: February 20th, 2022

Vivek Subramanian

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Vivek Subramanian